REMARKS

Claims 1-6, and 24-29 were presented for examination. Claims 1 and 24 were rejected under 35 U.S.C. §102 (b) as anticipated by U.S. Patent No. 5,854,801 to Yamada et al. ("Yamada"). Claims 2-6 and 25-29 were rejected under 35 U.S.C. §103 (a) as obvious over Yamada. Claims 1, 5 and 28 have been amended to fix typographical errors. No new matter is added. Claims 1-6, and 24-29 are presented for examination.

Finality of Office Action.

The pending Office Action was incorrectly made final. In the response to the Advisory Action issued on February 25, 2005, filed concurrently with a Request for Continued Examination (RCE), Applicant amended claims 1 and 24. The pending final Office Action was issued after receipt of the RCE. In a telephone interview with the Examiner on June 27, 2005, the Examiner acknowledged the Office Action was inappropriately made final and agreed to withdraw the finality of the Office Action. In an Advisory Action of August 8, 2005 the Examiner re-asserted the finality of the Office Action. In a telephone interview with the Examiner and the Examiner's Supervisor on October 13, 2005 The Examiner and Supervisor again acknowledged that the Office Action was inappropriately made final and agreed to withdraw the finality of the Office Action. Applicant would like to thank the Examiner and Supervisor for withdrawing the finality.

Rejections of claims 1 and 24 under 35 U.S.C. §102 (b)

Independent claim 1 and 24 were previously amended to include the limitation of "integrated circuit" and "semiconductor device", respectively. The claimed invention relates to built-in self-test (BIST) for testing embedded memory because external testing of the embedded memory is difficult due to the lack of direct connection between the input pins, output pins, and the embedded memory of the device. Yamada discusses a test pattern generation apparatus and method for SDRAM in various semiconductor devices to improve the conventional technology of testing semiconductor devices using semiconductor test systems (see Background Art).

Therefore, Yamada discusses an improvement of external test systems for testing semiconductor devices, which is very different from scope of the claimed invention.

Furthermore, Examiner's response to the amendment again asserts that "Yamada does not teach that all the elements are not on a integrated circuit and one of ordinary skill in the art would have recognized that testing an SRAM would high likely be done on a integrated circuit or a semiconductor device." The Examiner further cites In re Larson 144 USPQ 347 (CCPA 1965) in support of this assertion. Applicant respectfully submits that the Examiner is applying the wrong standard under 35 U.S. C. §102. The examiner is speculating as what is taught or suggested by Yamada. To anticipate claims 1 and 24 under 35 U.S. C. §102 a reference must *disclose* each and every element of the claims. The Examiner's statement effectively admits Yamada does not disclose each and every element. In the telephone interview with the Examiner and Supervisor on October 13, 2005, the Examiner and Supervisor acknowledged that the incorrect standard was being applied. Applicant would like to thank the Examiner and Supervisor for resolving this matter.

Thus, as set forth above, Applicant respectfully submits that Yamada does not disclose each and every element of independent claims 1 and 24, and looks forward to the Examiner withdrawing the rejections of claims 1 and 24.

Rejection of claims 1 and 24 under 35 U.S.C. §103(a)

As the rejection to claims 1 and 24 made by the Examiner under 35 U.S.C. §102 was in actuality a rejection under 35 U.S.C. §103, in the interest of furthering the prosecution, applicants will address the rejection to claims 1 and 24 as if there were properly rejected under 35 U.S.C. §103.

As stated above in regards to the 102 rejection, the claimed invention relates to built-in self-test (BIST) for testing embedded memory because external testing of the embedded memory is difficult due to the lack of direct connection between the input pins, output pins, and the embedded memory of the device. Claims 1 and 24 were previously amended to include the limitation of "integrated circuit" and "semiconductor device" respectively. In contrast, Yamada

discusses an improvement of external test systems for testing semiconductor devices, which is very different from scope of the claimed invention. As such, it would not have been obvious to include the teaching of Yamada into a built-in self test of internal memory because the implementation for external testing as set forth in Yamada is different from the implementation for the built-in self test of the present invention. Indeed, one of the problems overcome by the present invention is the lack of direct connection between the input pins, output pins, and the embedded memory of the device needed for external testing as taught in Yamada. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of claims 1 and 24.

Rejections of claims 2-6 and 25-29 under 35 U.S.C. §103(a)

Dependent claims 2-6, and 25-29 depends from one of independent claims 1 and 24. Yamada fails to teach or suggest an "integrated circuit" or "semiconductor device" as recited by claims 1 and 24. Yamada further fails to teach or suggest a conversion circuit comprising a memory storage device such a disclosed in 2-4 and 25-27. Yamada also fails to teach or suggest providing a test vector capable of detecting either spatial locality faults within the selected group of memory cells under test or coupling transitional faults between physically adjacent memory cells within the selected group of memory cells under test as set forth in claims 5, 6, 28 and 29.

The Examiner asserts that the conversion circuit of Yamada inherently has to have a temporary storage device. Applicant respectfully disagrees.

Yamada gives two examples of the predetermined logic circuit in Fig. 3 and Fig. 4. Furthermore, in col. 2, lines 26-30, lines 37-42, lines 56-60, col. 3 lines 6-11, and col. 4 lines 5-10, and lines 19-24, Yamada shows the different logic expressions of the logic circuit based on different embodiments. All these logic expressions are simple logic expressions that require only a few wires and a few gates to implement in hardware as illustrated in Fig. 3 and Fig. 4. Therefore, it is not inherent to have any temporary storage device to use with the conversion circuit as suggested by the Examiner. Therefore, it is not obvious for one ordinary skill in the art to add a storage device to Yamada and results in the present invention as claimed in dependent claims 2-4 and 25-27.

Examiner also appears to suggest that the address inversion scramble of Yamada substantially teaches providing a test vector capable of detecting either spatial locality faults within the selected group of memory cells under test or coupling transitional faults between physically adjacent memory cells within the selected group of memory cells under test. Applicant respectfully disagrees.

While there is an address inversion scramble for converting the address between the logical address and the physical address, there is no mention whatsoever of providing a test vector. In Yamada, the only disclosed outputs are addresses (row, column, or wrap). Thus, it would not be obvious to provide a test vector capable of detecting either spatial locality faults within the selected group of memory cells under test or coupling transitional faults between physically adjacent memory cells within the selected group of memory cells under test as claimed in dependent claims 5, 6, 28 and 29.

Claims 5, 6, 28 and 29 depends from one of independent claims 1 and 24, and include all the limitations of their corresponding independent claim. Therefore, Yamada does not teach or suggest all the limitations of claims 2-6, and 25-29. Furthermore, Yamada does not teach or suggest the subject matter set forth by claims 5, 6, 28 and 29. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of claims 2-6 and 25-29.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-041RCE from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

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